REMARKS

The following remarks are made in response to the Office Action mailed May 18, 2005. Claims 1-24 were rejected. Claims 1-24 and 28-31 are pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 103

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,763,478 (Bui) in view of U.S. Patent No. 6,336,166 (Kelly).

Applicant submits that it would not be obvious to one skilled in the art to combine the teachings of Bui either alone or in view of the secondary reference Kelly and arrive at the present invention of claims 1-24.

Bui discloses a computer system that includes a high performance clock frequency and a low performance clock frequency depending on whether battery or AC power is used. (See Bui, Abstract). When operating in low performance, FSB 105 bus frequency and memory bus 95 frequency will be set to 66 MHz. In high performance mode the two buses will operate at 100 MHz. (See Bui, column 5, lines 10-13.) The North Bridge ASIC 30 relays the clock frequency signal, either 66 MHz or 100 MHz, as a clock frequency signal represented by memory clock signal 75. The memory clock signal 75 is sent to the memory clock buffer 80, and the clock frequency is passed on as a memory clock signal 85 to SDRAM memory 90. (See Bui, column 5, lines 37-42).

Kelly discloses a computer memory access and control system, which includes a cache line buffers for ROM and an independent ROM bus. (See Kelly, column 1, lines 57-59). The computer memory access and control system also employs a ROM bus 205 that is separate and independent of the random access memory (RAM) buses, for example, RAM buses 210 and 215. (See Kelly, Figure 2, column 3, lines 22-30). With a separate ROM data path, that includes a full cache line buffer, memory access operations are more efficiently conducted because a RAM access (i.e., a read or write operation) and a ROM access (i.e., a read operation) can be executed concurrently (See Kelly, Abstract).

Applicant submits that Bui, either alone or in view of Kelly, fails to disclose, teach or suggest the invention of claim 1. Bui fails to disclose **a second memory bus.** See Examiner's Remarks Office Action, page 4. Further, Bui fails to disclose **a control system**

coupled to the first memory bus and the second memory bus, wherein the control system is configured to operate the first memory bus and the second memory bus at a first speed in the first power mode and a second speed different than the first speed in the second power mode.

Kelly also fails to disclose **a control system coupled to the first memory bus and the second memory bus, wherein the control system is configured to operate the first memory bus and the second memory bus at a first speed in the first power mode, and a second speed different than the first speed in the second power mode.** Kelly merely shows a ROM bus that is separate from the random access memory (RAM) bus. Accordingly, one could not combine the teachings of Bui either alone or in combination with the teachings of Kelly and arrive at the present invention of independent claim 1.

Further, neither Bui nor Kelly, teach or suggest **a control system configured to operate the first memory bus and the second memory bus at a first speed in the first power mode, and a second speed different than the first speed in the second power mode**. Again, Bui discloses ASIC 30 coupled to SD RAM memory 90 via memory bus 95. Kelly merely discloses a ROM bus 205 separate from RAM buses 210 and 215 to allow concurrent memory access. Kelly also fails to suggest operating **the first memory bus and the second memory bus at a first speed in the first power mode, and a second speed different from the first speed in the second power mode.** As such, it also would not be obvious to one skilled in the art to apply the teachings of Bui, in view of Kelly and arrive at the invention of independent claim 1. Similar limitations are included in independent claims 11, 17 and 21. Accordingly, Applicant requests that the above rejection of independent claims 1, 11, 17 and 21 under 35 U.S.C. § 103 be withdrawn.

Dependent claims 2-10, 12-16, 18-20 and 22-24 depend either directly or indirectly upon corresponding independent claims 1, 11, 17 and 21. Dependent claims 2-10, 12-16, 18-20 and 22-24 further define over the art of record. Accordingly, Applicant believes these dependent claims are also allowable.

Added New Claims

Claim 28-31 have been added. Applicant believes added claims 28-31 to be allowable over the art of record.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-25 and 28-31 are in form for allowance and are not taught or suggested by the cited references. Therefore, allowance of claims 1-25 and 28-31 is respectfully requested.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either Gregg W. Wisdom at Telephone No. (360) 212-8052, Facsimile No. (360) 212-3060 or Steven E. Dicke at Telephone No. (612) 573-2002, Facsimile No. (612) 573-0439. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 18 day of August, 2005.

By Steven E. Dicke
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